



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,081	09/23/2003	Jay Jie Lai	MSEMI.087A	1863
20995	7590	08/04/2005	EXAMINER	
KNOBBE MARTENS OLSON & BEAR LLP			WILSON, ALLAN R	
2040 MAIN STREET			ART UNIT	
FOURTEENTH FLOOR			PAPER NUMBER	
IRVINE, CA 92614			2815	

DATE MAILED: 08/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No. 10/669,081	Applicant(s) LAI ET AL.	
	Examiner Allan R. Wilson	Art Unit 2815	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 20 June 2005.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-24, 27 and 28 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1, 3-24, 27 and 28 is/are rejected.
- 7) ☒ Claim(s) 2 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 June 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Drawings*

The drawings filed on June 20, 2005 have been approved.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 4, 5, 7-13, 27 and 28 are rejected under 35 USC § 102(e) as being anticipated by U.S. Patent No. 6,703,689 to Wada.

With regards to claim 4, Wada illustrates in figures 1-15B, particularly figure 12, (entire document) an optoelectronic device 13 formed on a front side B of a semiconductor wafer 5, 6 in an integrated circuit fabrication process; and at least one electrical contact 22 on a backside A of the semiconductor wafer, wherein the electrical contact is electrically coupled to the optoelectronic device through a via 4 in the semiconductor wafer.

With regards to claim 5, Wada illustrates in fig. 12 the optoelectronic device 13 interfaces an optical system 106 with an electrical system (see next paragraph), and the front side of the semiconductor wafer is proximal to the optical system.

Art Unit: 2815

Regarding claims 5, 7-11, Wada illustrates in figures 13-15B, that the optoelectronic device 13 is formed above an electrical system (e.g. 1100 in FIG. 13) by means of solder bump connections 24 such that the backside of the chip is proximal the electrical system. The board (not shown) on which the optoelectronic chip is mounted reads on a carrier or chip as they are merely labels which do not structurally distinguish over Wada.

With regards to claims 12, Wada illustrates in FIG. 12 an array by the continuation on the left and right sides.

With regards to claim 13, Wada discloses in at least col. 5, lines 64, the optoelectronic devices 13 are photo detectors (photoreceivers).

With regards to claims 27 and 28, the examiner had to assume what the product would be by the process claimed. For example, it was assumed that the product was the optoelectronic device. The claim that it was "formed by epitaxial growth" was not considered to have full patentable weight. A "product by process" claim is directed to the product per se, no matter how actually made, MPEP 2113 "Product-by-Process Claims," In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90; In re Marosi et al, 218 USPQ 289; and particularly In re Thorpe, 227 USPQ 964, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 3 and 15-17 are rejected under 35 USC § 103 (a) as being unpatentable over Wada as applied to claim 4 above, and further in view of U.S. Patent No. 4,491,983 to Pinnow et al. ("Pinnow").

With regards to claims 1 and 3, Wada is discussed above, it does not show a PIN photodiode coupled to a transimpedance amplifier. Pinnow illustrates in figure 3a and discloses in col. 6, lines 6-10 a PIN photodiode 63 coupled to a transimpedance amplifier 64 to the anode and cathode (inherent). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have a high speed PIN photodiode coupled to a wide band transimpedance amplifier in accordance with Wada to provide an integrated connection.

With regards to claims 15 and 17, Wada illustrates in FIG. 12 a photoreceiver 13 formed on a front side of a semiconductor wafer 6 in fabrication of an integrated circuit; a first contact 22 on a back side of the semiconductor wafer, wherein the first contact is electrically coupled to an anode (inherent) of the photoreceiver by a first via 4 through a substrate-of the semiconductor wafer; and a second contact 22 on the back side of the semiconductor wafer, wherein the second contact is electrically coupled to a cathode of the photoreceiver by a second via 4 through the semiconductor wafer. Wada does not show the photoreceiver is a photodiode. Pinnow illustrates

Art Unit: 2815

in FIG. 3a a PIN photodiode. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have PIN photodiode for its' high speed (Pinnow col. 6, line 6).

With regards to claim 16, Wada discloses in col. 6, lines 51-53, the semiconductor wafer 5 is a Si material.

Claims 6 and 18 are rejected under 35 USC § 103 (a) as being unpatentable over Wada as applied to claim 4 above, and further in view of U.S. Patent No. 6,686,580 to Glenn et al. ("Glenn").

With regards to claim 18, Wada is discussed above, it does not show "the optoelectronic device interfaces an optical system with an electrical system, and the front side of the semiconductor wafer is proximal to the optical system." Glenn illustrates in figure 6 a optoelectronic device 106 interfaces an optical system 560C with an electrical system (not shown, col. 3 lines 60-62, a printed circuit board inherently has an electrical system) and the front side of the semiconductor wafer is proximal to the optical system. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have Wada connected to an optical system to provide the light gathering of a wide angle lens.

Regarding claim 6, Glenn teaches that the optoelectronic device has an aperture 502 for communication with an optical system 560C, and the aperture is proximal the optical system (as shown in figure 6).

Claims 14, 23 and 24 are rejected under 35 USC § 103 (a) as being unpatentable over Wada as applied to claim 12 above, and further in view of U.S. Patent No. 6,614,103 to

Art Unit: 2815

Durocher et al. ("Durocher"). Wada is discussed above, it does not show "light emitting."

Durocher teach that the optoelectronic devices may be photo detectors, light emitting devices (LEDs) or laser diodes which includes VCSELs (col. 9, lines 36-42). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have an array to provide an improved light emitting intensity.

Regarding claims 19-22, Wada in view of Pinnow taught the device of claim 15 but did not expressly teach the device was further bumped connected or coupled to a chip carrier or electronic receiver. However, these limitations are considered obvious over Durocher, in light of Wada and Pinnow. It is obvious that the device of Durocher, when using photodiodes as the optoelectronic devices 59, must be coupled to an external device, be it a chip carrier or other electronic receiver, such that use may be made of the light signal received by element 59. Durocher also teaches that the top of the photodiode 59 is exposed above the chip 41, and would also be exposed above any carrier on which the chip is placed. Finally, Pinnow makes obvious the use of a transimpedance amplifier to be coupled to a photodiode.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

Art Unit: 2815

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

*Allowable Subject Matter*

Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

*Response to Arguments*

Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

*Conclusion*

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,



Art Unit: 2815

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from an examiner should be directed to Primary Examiner Allan Wilson whose telephone number is (571) 272-1738. Examiner Wilson can normally be reached 7:00-4:00 Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Allan R. Wilson  
Primary Examiner  
August 3, 2005